STRUCTURE AND METHOD FOR ENHANCED PERFORMANCE IN SEMICONDUCTOR SUBSTRATES

FIELD OF THE INVENTION

Embodiments of the present invention relate to the field of semiconductor devices. In particular, embodiments of the present invention relate to the electrical and thermal resistances of semiconductor device substrates.

BACKGROUND ART

Prior Art FIG. **1** shows a general example of a semiconductor device **100**. The semiconductor device **100** has a substrate **105** with a back side metal layer **110**, a first epitaxial layer **115**, and a second epitaxial layer **120**. A number of active regions **125** are disposed in the second epitaxial region **120**. The active regions **125** contain circuit elements such as transistors or diodes that conduct electric current and dissipate heat. Examples of transistors are bipolar junction transistors (BJTs), metal-oxide field effect transistors (MOSFETs), and junction field effect transistors (JFETs).

The back side metal layer is commonly used to provide an electrical contact (e.g., ground) to the substrate **105** and to provide a solderable surface for mounting the device. For the semiconductor device **100**, there is a thermal/electrical resistance R associated with the substrate **105**. For vertical power devices such as field effect transistors (FETs) that utilize layer **110** as a source contact, the resistance R can be a significant fraction of the device on resistance R_{ds}-on.

The resistance R can be reduced by reducing the thickness of the substrate **105**. However, wafer handling considerations and electrical requirements limit the reduction in thickness that may be applied to the substrate **105** and epitaxial layer **115**.

Prior Art FIG. **2**A shows an example of a complementary metal-oxide semiconductor (CMOS) inverter circuit **200** fabricated on a p-type substrate **205**. A p-channel field effect transistor (PFET) **215** resides in an N-well **210** and is coupled to an n-channel field effect (NFET) transistor **220**. The CMOS inverter circuit **200** is a basic building block for digital logic circuits.

Prior Art FIG. **2**B shows an equivalent circuit **201** that includes parasitic bipolar transistors Q**1** and Q**2** that are derived from the p-n junctions associated with the inverter circuit **200**. During normal operation of the inverter **200** the parasitic transistors Q**1** and Q**2** are off. However, if a transient voltage spike or other event produces a large current through $R_{substrate}$, the voltage drop across $R_{substrate}$ will be sufficient to turn on Q**2** and cause a current flow through R_{well}. If the voltage drop across R_{well} is large enough to turn on Q**1**, latchup occurs wherein a self sustained low resistance path between V_{dd} and GND is produced.

FIG. **2**C shows **2**C shows a schematic representation **202** of the substrate bulk resistance $R_{substrate}$ associated with the equivalent circuit **201** of FIG. **2**B. The bulk resistance $R_{substrate}$ is distributed in the region between the N-well **210** and the NFET **220**. In contrast to the resistance R of a vertical device, the resistance $R_{substrate}$ is part of a lateral current path.

Thus, in conventional semiconductor substrates there is frequently a bulk region that either contributes to undesirable resistance in operational electrical or thermal paths, or provides an additional current path with undesirable properties.

SUMMARY OF INVENTION

Accordingly, embodiments of the present invention are directed toward an etched substrate structure that may augmented by conductive material to provide enhanced electrical and thermal performance, or aligned with die separation lines to facilitate die separation.

In an embodiment of the present invention, a semiconductor device substrate comprising active regions defined on a top surface is masked and etched to define a pattern of blind features in a bottom surface of the substrate. A conductive material is then deposited on the surface of the blind features. The replacement of semiconductor material with the conductive material lowers the resistance between the active elements on the top surface and the bottom surface.

In another embodiment of the present invention, a semiconductor device substrate comprising a circuit susceptible to latchup on a top surface is etched and metallized to reduce the substrate bulk resistance, thereby reducing the susceptibility to latchup.

In a further embodiment, a semiconductor substrate is provided with a pattern of grooves on a bottom surface. The pattern of grooves is positioned opposite to a scribe street pattern on the top side of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Prior Art FIG. **1** shows a general schematic for thermal and electrical resistances in a semiconductor device substrate.

Prior Art FIG. **2**A shows an example of a semiconductor device that is susceptible to latchup.

Prior Art FIG. **2**B shows a schematic diagram for the device of FIG. **2**A.

Prior Art FIG. **2**C shows a schematic representation of the substrate bulk resistance associated with the circuit of FIG. **2**B.

FIG. **3**A shows a semiconductor device substrate with partially filled blind features in accordance with an embodiment of the present invention.

FIG. **3**B shows a semiconductor device substrate with street-aligned grooves in accordance with an embodiment of the present invention.

FIG. **4** shows a CMOS device with a reduced $R_{substrate}$ in accordance with an embodiment of the present invention.

FIG. **5** shows a flow diagram for a method of decreasing the electrical resistance and/or thermal resistance of a semiconductor device substrate in accordance with an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the present invention, a structure and method for enhanced performance in semiconductor substrates, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known circuits and components have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

FIG. **3**A shows a semiconductor device **300** in accordance with an embodiment of the present invention. The active regions **125**, epitaxial layers **115** and **120** are similar to those